

REMARKS

The Office Action dated February 15, 2005 has been received and carefully considered. In this response, claims 1-10, 16, 20, 21, 24-27, 29, 34 and 36 have been amended. Support for the amendments to the claims may be found in the specification and figures as originally filed. Entry thereof and reconsideration of the outstanding rejections therefore is respectfully requested.

Telephonic Interview of May 12, 2005

At the outset, the undersigned notes with appreciation the courtesies extended by the Examiner during the telephonic interview of May 12, 2005 (hereinafter, "the Interview"). As noted by the Applicant's representative during the Interview, and as acknowledged by the Examiner, Nitta (U.S. Patent No. 6,625,207) does not disclose or suggest that different color depths are used based on similarities or differences between display data. The Applicant respectfully submits that Nitta fails to disclose or suggest that different numbers of bits are used to represent color information of display data for similar reasons. Thus, the amendments to claims 20 and 34 as provided herein would overcome the rejections of claims 20 and 34 in view of Nitta.

Moreover, the Applicant's representative noted that Nitta fails to disclose or suggest that display data is provided at different frame rates and Nitta therefore fails to disclose or suggest each and every feature of claims 1 and 28. The Examiner reasoned that Nitta disclosed changing a "frame rate" because the bit rate between the transceiver 100 and the receiver 200 of Nitta could change depending on whether the 3-bit data or the 24-bit data was transmitted and therefore the number of "data frames" per unit time could change. However, as noted by the Applicant's representative, the Examiner's interpretation of the term "frame rate" is inconsistent both with the term as understood by one of ordinary skill in the art and as taught by the present application. The term "frame rate" does not refer to a bit rate or to a number of packetized data frames per second. Instead, as understood in the art, the term frame rate refers to the number of image frames provided for display per unit time (typically represented as frames-per-second or fps). As an exemplary exercise, the Applicant's representative obtained a number of definitions for the term "frame rate" from the on-line search engine at <http://www.google.com>. The

resulting definitions are provided below as Appendix A. As the Examiner will note, the overwhelming majority of these definitions for "frame rate" essentially provide that a frame rate is the rate or number of image frames per second. The Applicants therefore respectfully submit that the Examiner's interpretation of frame rate is improper.

Anticipation Rejection of Claims 1, 5-23, 27-30, 32, 33 and 35-41

At page 2 of the Office Action, claims 1, 5-23, 27-30, 32, 33 and 35-41 were rejected under 35 U.S.C. Section 102(e) as being anticipated by Nitta (U.S. Patent No. 6,625,207). This rejection is respectfully traversed.

Claim 1, from which claims 5-19 depend, recites the features of providing display data to a display port at a first frame rate when the first display content is different from the second display content and providing display data to the display port at a second frame rate when the first display content is different from the second display content, wherein the second frame rate is less than the first frame rate. Claim 28, from which claims 29, 30, 32, 33 and 35-41 depend, recites the features of a display module to alter a frame rate for providing display data to a display port, wherein said frame rate is based on the comparison performed by a content analyzer.

As noted during the Interview and as discussed above, Nitta fails to disclose or suggest changing a frame rate (as the term is understood in the art and as used by the present application) of display data provided to a display port. As provided by the Abstract of Nitta and as illustrated by Fig. 2 of Nitta, Nitta teaches that when the display data in a holding circuit from a previous transmission is the same as the display data to be transmitted (i.e., having the same bit values), the display data is encoded and transmitted as 3-bit display data rather than the full 24-bit display data. As FIG. 2 and the cited passages of Nitta disclose, the comparison of n-bit parallel data (e.g., the 24-bit example provided by Nitta) is performed. As also disclosed by Nitta, this 24-bit parallel data may represent the red (R), green (B) and blue values (eight bits each) of a single pixel. Thus, Nitta discloses comparison of display data on a pixel-by-pixel basis. *See Nitta*, col. 5, line 61- col. 6, line 5. When the display data is the same as the data in the holding circuit, the display data is encoded into a 3-bit value (see the encoder 120, Fig. 2) and the encoded 3-bit data value is provided in place of the full 24-bit value data. Thus, based on the teachings of Nitta and the Examiner's comments, it appears that the Examiner considers that the selection between a 3-

bit encoded value or a 24-bit value to represent the output display data based on the pixel-by-pixel comparison is the same as selecting between a first frame rate and a second frame rate based on a comparison of display contents. However, as noted above, one of ordinary skill in the art will appreciate that a frame rate and a "bit-rate" (as the Examiner summarizes the technique of Nitta) are not the same or equivalent. Moreover, as disclosed at FIG. 5 and, for example, col. 11, lines 27-31, the receiver circuit 200 at the display receives the transmitted data (either in 3-bit or 24-bit form) and, if in 3-bit form, converts the 3-bit data back to the original 24-bit value using the holding circuit 210. Thus, the overall display data rate to the display stays the same from the viewpoint of the display device.

Consequently, Nitta necessarily fails to disclose or suggest the features of providing display data to a display port at a first frame rate when the first display content is different from the second display content and providing display data to the display port at a second frame rate when the first display content is different from the second display content, wherein the second frame rate is less than the first frame rate, as recited by claim 1 or the features of a display module to alter a frame rate for providing display data to a display port, wherein said frame rate is based on the comparison performed by a content analyzer as recited by claim 28. Accordingly, the Office Action fails to establish that Nitta discloses or suggests each and every feature of claims 1 and 28, as well as claims 5-19 and 29, 30, 32, 33 and 35-41 at least by virtue of their dependency from one of claims 1 or 28. Moreover these claims recite additional features not disclosed by Nitta.

Claim 20, from which claims 22, 23 and 27 depend, has been amended to recite the features of using a first number of bits to represent color information of display data, when the first display content is different from the second display content and using a second number of bits to represent color information of display data, when the first display content is substantially the same as the second display content, wherein the second number of bits is less than the first number of bits. Claim 34, from which claims 35-41 depend, has been amended to recite the features of a display module to alter a number of bits used to represent color information of display data, wherein said number of bits is based on the comparison performed by said content analyzer. As acknowledged by the Examiner during the Interview, Nitta fails to disclose that different color depths may be used. The Applicants respectfully submit that Nitta also fails to disclose that different numbers of bits may be used to represent color information of display data

for similar reasons, so Nitta necessarily fails to disclose or suggest each and every feature of claims 20 and 34, as well as each and every feature of claims 22, 23, 27 and 35-41 at least by virtue of their dependency from one of claims 20 or 34. Moreover, these claims recite additional features not disclosed by Nitta.

In view of the foregoing, it is respectfully submitted that the anticipation rejection of claims 1, 5-23, 27-30, 32, 33 and 35-41 is improper at this time and the withdrawal of this rejection therefore is respectfully requested.

Obviousness Rejection of Claims 2-4, 24-26, 31 and 34

At page 6 of the Office Action, claims 2-4, 24-26, 31 and 34 were rejected under 35 U.S.C. Section 103(a) as being unpatentable over Nitta in view of Mirov (U.S. Patent No. 6,691, 215). This rejection is respectfully traversed.

As noted above, Nitta fails to disclose or suggest the features of claim 1 of providing display data to a display port at a first frame rate when the first display content is different from the second display content and providing display data to the display port at a second frame rate when the first display content is different from the second display content, wherein the second frame rate is less than the first frame rate. Nitta also fails to disclose or suggest the features of claim 28 of recites similar features of a display module to alter a frame rate for providing display data to a display port, wherein said frame rate is based on the comparison performed by a content analyzer. The Office Action does not assert that Mirov discloses these features, nor are these features found in Mirov. Accordingly, the proposed combination of Nitta and Mirov necessarily fails to disclose or suggest each and every feature of claims 2-4 and 31 at least by virtue of their dependency from claims 1 and 28, respectively. Moreover, these claims recite additional features that are neither disclosed nor suggested by Nitta or Mirov.

For example, claim 4 recites the features of wherein enabling a second clock rate includes disabling a phase locked loop. Although the Examiner relies on Mirov as allegedly disclosing these features, the Applicants respectfully submit that Mirov teaches merely *bypassing* the PLL rather than *disabling* the PLL as provided by claim 4. *See Mirov*, Figure 10 (note the "PLL BYPASS" signal input to the multiplexer 1010, which receives as its inputs the clock in directly

or the output of the VCO 1004); *see also Mirov*, col. 16, lines 9-40 (describing how the PLL 904 may be bypassed using the multiplexer 101 and the PLL BYPASS signal).

As also noted above, Nitta fails to disclose or suggest the features of claim 20 of using a first number of bits to represent color information of display data, when the first display content is different from the second display content and using a second number of bits to represent color information of display data, when the first display content is substantially the same as the second display content, wherein the second number of bits is less than the first number of bits. Nitta also fails to disclose or suggest the features of claim 34 of a display module to alter a number of bits used to represent color information of display data, wherein said number of bits is based on the comparison performed by said content analyzer. The Office Action does not assert that *Mirov* teaches these features, nor are these features found in *Mirov*. Accordingly, the proposed combination of Nitta and *Mirov* fails to disclose or suggest each and every feature of claim 34, as well as each and every feature of claims 24-26 at least by virtue of their dependency from claim 20.

For example, as noted above with respect to claim 4, *Mirov* fails to disclose or suggest disabling a PLL, so *Mirov* necessarily fails to disclose or suggest the features of wherein enabling a second clock rate includes disabling a phase locked loop as recited by claim 26.

In view of the foregoing, it is respectfully submitted that the obviousness rejection of claims 2-4, 24-26, 31 and 34 is improper and the withdrawal of this rejection therefore is respectfully requested.


Conclusion

It is respectfully submitted that the present application is in condition for allowance, and an early indication of the same is courteously solicited. The Examiner is respectfully requested to contact the undersigned by telephone at the below listed telephone number in order to expedite resolution of any issues and to expedite passage of the present application to issue, if any comments, questions, or suggestions arise in connection with the present application.

The Commissioner is hereby authorized to charge any fees that may be required, or credit any overpayment, to Deposit Account Number 50-0441.

Respectfully submitted,

13 May 2005
Date


Ryan S. Davidson, Reg. No. 51,596,
TOLER, LARSON & ABEL, L.L.P.
5000 Plaza On The Lake, Suite 265
Austin, Texas 78746
(512) 327-5515 (phone) (512) 327-5452 (fax)